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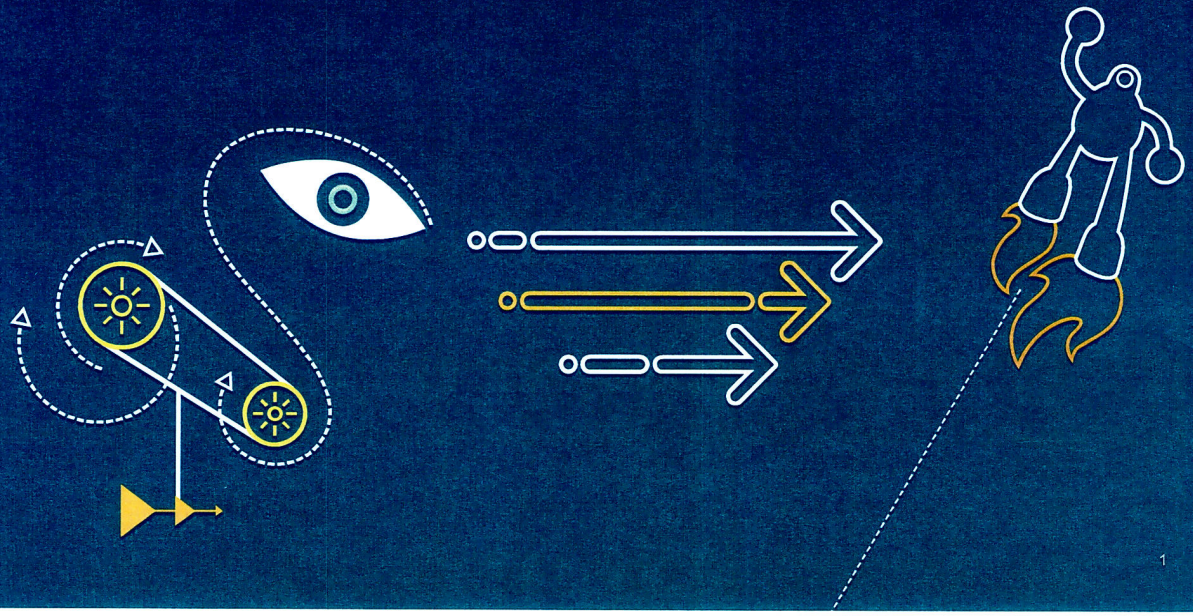
Overview of Qualcomm Hexagon DSP (QDSP6)

QUALCOMM®



QUALCOMM in Austin

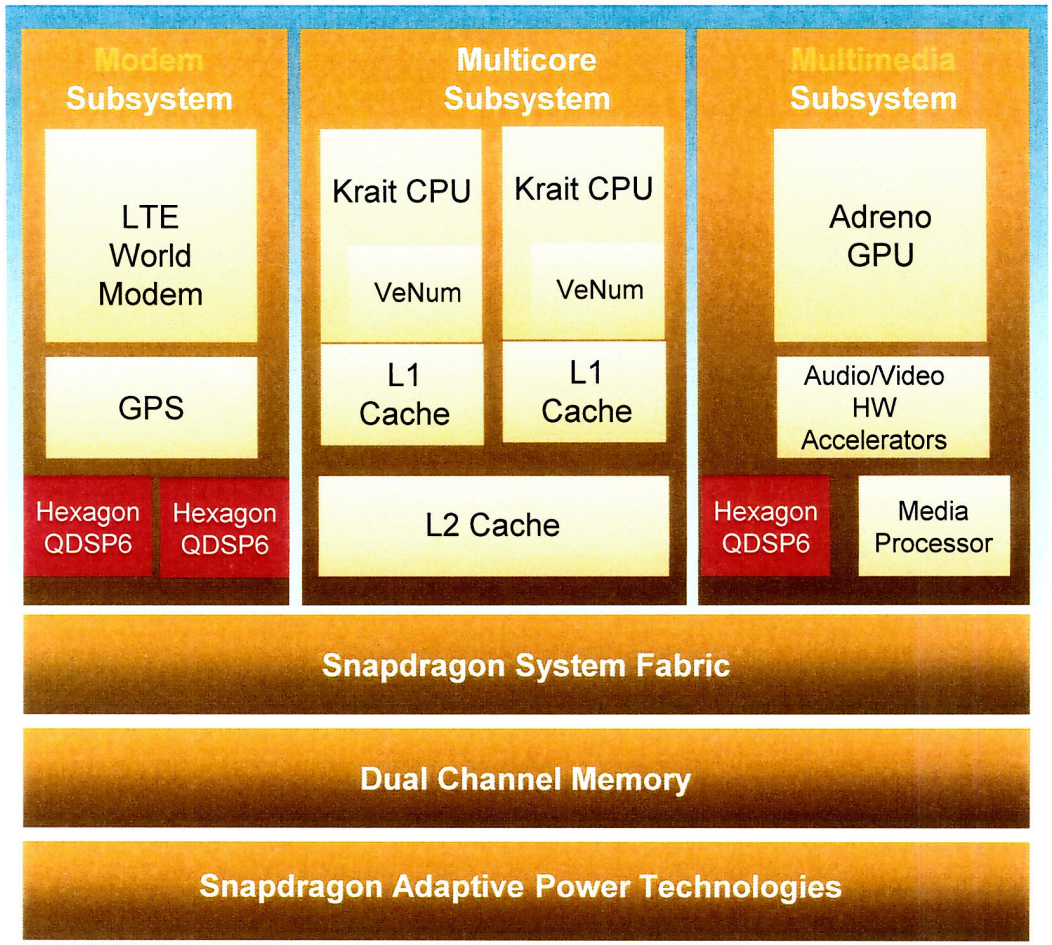
- Qualcomm Technologies Inc. (QTI) is the
  - Largest Fabless Manufacturer Since 2003
    - Overall Semiconductor Industry Ranking in 2012: 3rd
  - the Largest Global Manufacturer of Wireless Baseband ("Cell Phone") Chips
    - QTI Sells ~170 Million Chipsets / Quarter
- Willie Anderson Leads QTI Austin Design Center
  - QTI Austin Has Been Designing DSPs Since 2004
  - 5 DSPs Designed in Austin, Now in Dozens of Chips

Source: IHS iSuppli, IC Insights' Strategic Review Database

Qualcomm Hexagon™ DSP

Robust Capability + Superior Power Efficiency

Snapdragon™ S4: MSM8960 Block Diagram



Hexagon Processor Core-level System Architecture

- 4-issue VLIW with Interleave Hardware Threading
  - 1~4+ instructions per cycle. Managed by software
- Dual 64-bit load/store units
  - 8/16/32/64-bit ld/st, 32b scalar
- Dual 64-bit vector units
  - 8/16/32/64-bit vectorized MPY/ALU/SHIFT/SP, Permute, Bit manipulation
  - 16 8x8, Eight 16x16, Four 16x32, Two 32x32 or SP FP MACs/cycle
- Unified vector/scalar/floating-point register
- Compound instructions
  - Fuse simple instructions
- Novel data-flow packets
  - Intra-packet data forwarding enables single cycle load-compare-branch

Execution Unit of Hexagon

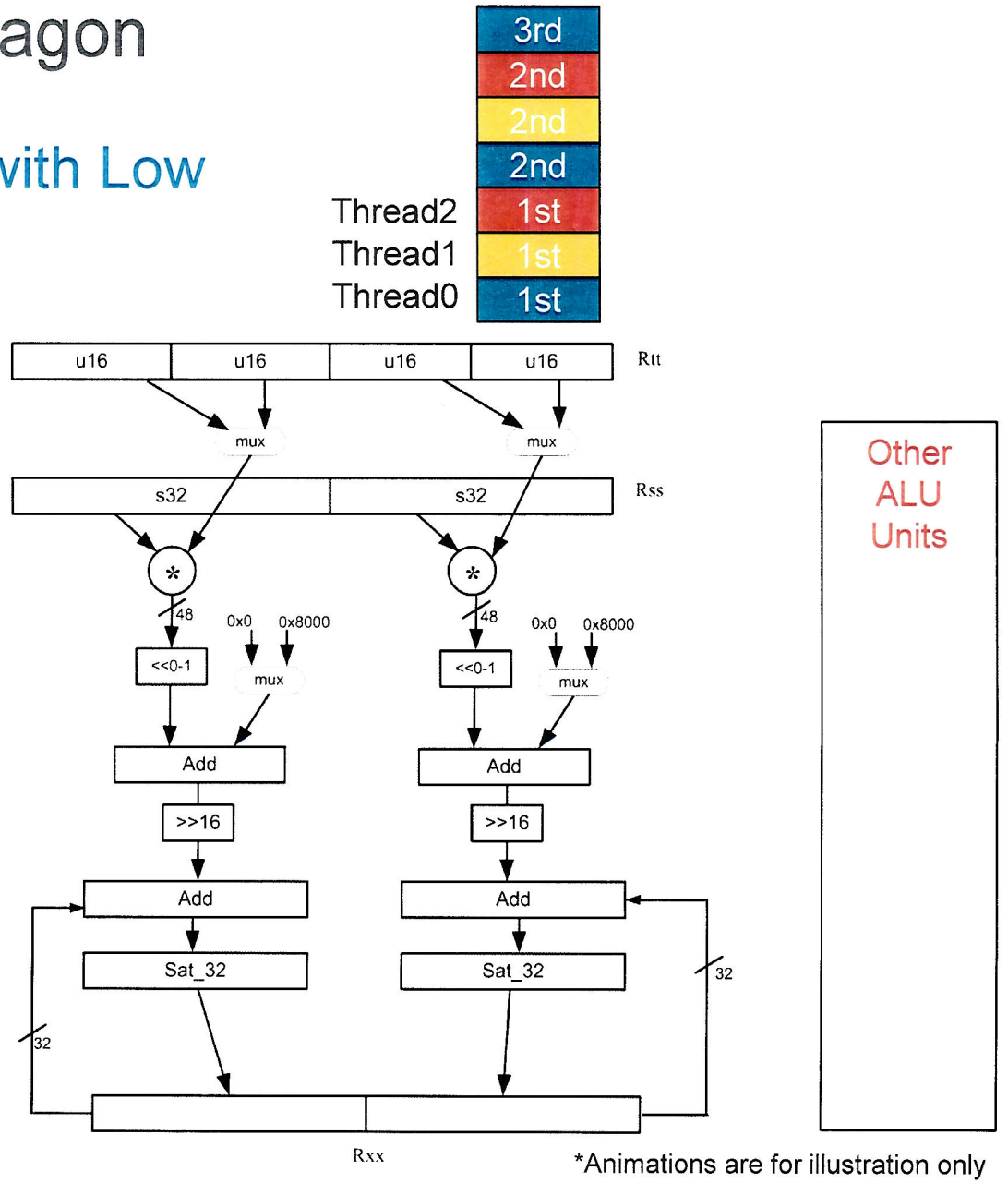
Powerful Execution Unit with Low Energy Consumption

- Supported datatype:
  - integer (signed/unsigned), fractional, and complex numbers
  - Single precision floating point numbers
- Supported instructions in both scalar and vector forms
  - Basic arithmetic instructions
  - Floating point (compliant to IEEE 754-2008) and FP ⟷ Integer convert instructions
  - Hundreds of compound instructions
  - Special-purpose instructions
    - Focus on communications, audio, video, imaging

Execution Unit of Hexagon

Powerful Execution Unit with Low Energy Consumption

- Hardware multitheading enables complex and compound instructions to be run in hardware



*Animations are for illustration only

Performance from Work/Cycle, not Frequency

Fixed-Point Processors (single core)	Clock Rate (MHz) per Thread max	BDTImark2000 BDTIsimMark2000 max	BDTImark2000 per MHz max
Qualcomm Hexagon V2 (1 thread)	100	1,550	15.5
Qualcomm Hexagon V2 (6 threads)	600	9,300	15.5
Qualcomm Hexagon V4 & V5 (1 thread)	233	4,220	**18.1**
Qualcomm Hexagon V4 & V5 (3 threads)	700	12,660	**18.1**
TI TMS320C64x+	1,200	13,170	11.0
TI TMS320C66x	1,500	20,030	13.4
CEVA CEVA-X1620	330	2,660	8.1
CEVA TeakLite-III	335	2,140	6.4
Tensilica ConnX 545CK	245	4,070	16.6

- Hexagon processor
  - Architecture evolution to deliver performance at low power
  - Elimination of power-hungry operations
    - Speculation: branch prediction, parallel tag/data caches, etc.
    - Memory stalls: cache prefetch, out-of-order execution
    - High clock rate design methods
- Results: More work at lower clock
  - Lower energy for same performance

Source: Berkeley Design Technology, Inc.

Conclusion

- Power consumption and Performance are important in mobile space
- By working with GPU and CPU seamlessly, Hexagon DSP is designed to provides the low energy footprint while enables massive data and control processing power

Acknowledgement

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